

**SYSTEM AND METHOD INCLUDING DISTRIBUTED INSTRUCTION
BUFFERS
HOLDING A SECOND INSTRUCTION FORM**

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ABSTRACT OF THE INVENTION

A system and method is provided for processing a first instruction set and a second instruction set in a single processor. The method includes storing a plurality of control signals in a plurality of buffers proximate to a plurality of execution units, wherein the control signals are predecoded instructions of the second instruction set, executing an instruction of the first instruction set in response to a branch instruction of the first instruction set, and executing the control signals for an instruction of the second instruction set in response to a branch instruction of the second instruction set.

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